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In re Application of :

Shoso SHINGUBARA et al. :

Serial No. 10/809,681 : Group Art Unit: 1762

Filed: March 26, 2004 : Examiner: Katherine A. Bareford

For: METHOD OF MANUFACTURING MULTI-LAYER INTERCONNECTION STRUCTURE

VERIFICATION OF ENGLISH TRANSLATION

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

I, Haruo NAKANO , declare that I am conversant in both the Japanese and English languages and that the English translation as attached hereto is an accurate translation of Japanese Patent Application No. 2003-120338 filed on April 24, 2003.

Signed this 21st day of June, 2007

Haruo Nakano

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Applicant(s) : Semiconductor Technology Academic Research Center

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Commissioner,
Patent Office Yasuo IMAI (seal)

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Item:	Specification	1 copy
Item:	Drawings	1 copy
Item:	Abstract	1 copy

Request for Proof Transmission: Yes

[Document Name] SPECIFICATION

[Title of the Invention] METHOD OF MANUFACTURING MULTI-LAYER INTERCONNECTION STRUCTURE

[Scope of the Claims]

[Claim 1] A method of manufacturing an embedded multi-layer interconnection structure, comprising:

a step of forming a hole portion in an insulation layer;

a barrier metal film forming step of forming a barrier metal film which is comprised mainly of tantalum and nitrogen in such a manner that said barrier metal film covers at least an inner wall of said hole portion;

a removal step of removing an oxide film formed on a surface of said barrier metal film; and

an electroless plating step of immersing said barrier metal film in a plating liquid containing copper and thereby forming an electroless copper plating film on said barrier metal film,

characterized in that an element composition ratio (N / Ta) of nitrogen to tantalum contained in said barrier metal film is 0.3 or higher but 1.5 or lower.

[Claim 2] The manufacturing method of claim 1, characterized in that said element composition ratio (N / Ta) is 0.3 or higher but 1.0 or lower.

[Claim 3] The manufacturing method of claim 1 or 2, characterized in that said barrier metal film forming step is a plasma nitriding step at which nitrogen plasma is irradiated upon a surface of a film which is comprised mainly of tantalum and accordingly nitriding tantalum.

[Claim 4] The manufacturing method of claim 1 or 2, characterized in that said removal step is such a step at which said oxide film is removed and said barrier metal film is left in such a manner that said barrier metal film entirely covers said inner wall of said hole portion.

[Claim 5] The manufacturing method of claim 1 or 2, characterized in that said removal step is such a step at which said barrier metal film is immersed in a mixture of a hydrofluoric acid and a nitric acid or a diluent of a hydrofluoric acid and said oxide film

is selectively removed.

[Claim 6] The manufacturing method of claim 1 or 2, characterized in that said electroless plating step is such a step at which said barrier metal film is immersed in a plating liquid which uses a glyoxylic acid as a reducer.

[Claim 7] The manufacturing method of any one of claims 1 through 6, characterized in further comprising a step at which, through electrolytic plating which uses said electroless copper plating film as a seed layer, an electroless copper plating film is formed on said electroless copper plating film.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a method of manufacturing a multi-layer interconnection structure, and more particularly, to a method of manufacturing an embedded multi-layer interconnection structure.

[0002]

[Prior Art]

As a device topography has become finer and the aspect ratio of a via hole in which a wire is buried has accordingly increased, development of a void within the via hole has arisen as a problem with a method of manufacturing an embedded multi-layer interconnection structure which uses a conventional darmascene process.

To deal with this, a displacement plating method has been proposed according to which copper plating is provided without using a catalyst such as Pd on a TaN barrier layer formed inside a via hole (See the non-patent document 1 for instance.).

[0003]

A displacement plating method utilizes that in a plating solution, when the oxidation-reduction potential of underlying metal is lower than the oxidation-reduction potential of copper which is contained in the plating solution, ions of the underlying metal are oxidized and accordingly dissolve in the plating solution, and instead, copper ions within the plating solution are reduced and deposited.

In the event that TaN is used as underlying metal (barrier metal)

of a multi-layer interconnection structure, mere immersion of the underlying metal in an electroless copper plating liquid causes plating of copper by means of displacement. Further, since autocatalytic plating is possible after deposition of copper, it is possible to deposit an electroless copper plating film on the underlying metal through extremely simple steps.

[0004]

Fig. 3 shows cross sectional views of conventional steps of manufacturing a multi-layer interconnection structure which uses a displacement plating method. These manufacturing steps include the following steps 1 through 5.

[0005]

Step 1: As shown in Fig. 3(a), an inter-layer insulation film 3 of silicon oxide is formed on an inter-layer insulation film 1 which is made of silicon oxide and comprises a lower-layer wire 2. Next, the inter-layer insulation film 3 is etched, thereby forming a via hole (hole portion) 4. Further, through sputtering, a barrier metal film (underlying metal) 15 of TaN is formed on the entire surface.

[0006]

Step 2: As shown in Fig. 3(b), the barrier metal film 15 is exposed to atmosphere, whereby a surface of the barrier metal film 15 is oxidized and a natural oxide film 16 of TaN is formed.

[0007]

Step 3: As shown in Fig. 3(c), the natural oxide film 16 formed on the surface of the barrier metal film 15 is removed through etching.

[0008]

Step 4: As shown in Fig. 3(d), by means of immersion into a plating liquid which contains copper, an electroless copper plating film 17 is formed by a displacement plating method.

[0009]

Step 5: As shown in Fig. 3(e), further, by an electrolytic plating method, an electrolytic copper plating film 18 is formed. Through these steps, a multi-layer interconnection structure 200 is completed.

[0010]

[Non-patent Document 1]

Zenglin Wang, Hiroyuki Sakaue, Shoso Shingubara and Takayuki Takahagi "Electroless Plating of Cu Initiated by Displacement Reaction on Metal-Nitride Diffusion Barriers" Electrochem. Solid-State Letters, 6 (3) (2003) C38-C41

[0011]

[Problems to be Solved by the Invention]

However, even when a displacement plating method is used, there arises a problem of a void within a via hole as a device topography becomes finer and the line width of a wire becomes as narrow as 100 nm or less for instance. Noting this, the inventors of the present invention studied the causes of a void and learned the following.

That is, as a device topography becomes finer, the film thickness of the barrier metal film 15 decreases. Because of this, at the step 2, the barrier metal film 15 located at a side wall where the film thickness is thinner than at a bottom surface turns entirely into the natural oxide film 16. Therefore, through removal of the natural oxide film 16 at the step 3, no barrier metal film 15 will remain on the side wall.

As a result, any plating film is not formed on a side wall of the via hole 4 at the step 4 which is an electroless plating step, which in turn will causes a void 19.

[0012]

According to the ITRS semiconductor roadmap for example, the film thickness of a barrier metal film will be 8 nm for the 65nm line-width generation and will be 5 nm for the 45nm line-width generation. Hence, if the film thickness of the natural oxide film (oxygen-rich layer) 16 formed on the surface of the barrier metal film 15 of TaN exceeds 5 nm, a void will be created. In the event that the barrier metal film 15 is formed by a sputtering method in particular, the film thickness of the barrier metal film 15 located at the side wall of the via hole is thin, and therefore, development of a void will be remarkable.

[0013]

An object of the present invention is therefore to provide a method of manufacturing a multi-layer interconnection structure for use in an LSI comprising finely patterned wires, according to which

a natural oxide film formed on a surface of a barrier metal film is thin and development of a void is prevented.

[0014]

[Means to Solve the Problem]

The present invention is directed to a method of manufacturing an embedded multi-layer interconnection structure, comprising: a step of forming a hole portion in an insulation layer; a barrier metal film forming step of forming a barrier metal film which is comprised mainly of tantalum and nitrogen in such a manner that the barrier metal film covers at least an inner wall of the hole portion; a removal step of removing an oxide film formed on a surface of the barrier metal film; and an electroless plating step of immersing the barrier metal film in a plating liquid containing copper and thereby forming an electroless copper plating film on the barrier metal film, characterized in that an element composition ratio (N / Ta) of nitrogen to tantalum contained in the barrier metal film is 0.3 or higher but 1.5 or lower.

Use of the barrier metal film having such an element composition ratio allows that the film thickness of the natural oxide film formed on the barrier metal film is as thin as 1 nm or less for instance. In addition, a favorable resistor value as a wiring layer is obtained.

[0015]

The element composition ratio (N / Ta) is preferably 0.3 or higher but 1.0 or lower.

[0016]

The barrier metal film forming step may be a plasma nitriding step at which nitrogen plasma is irradiated upon a surface of a film which is comprised mainly of tantalum and accordingly nitriding tantalum.

[0017]

The removal step is such a step at which the oxide film is removed and the barrier metal film is left in such a manner that the barrier metal film entirely covers the inner wall of the hole portion. As the barrier metal film is left on the entire surface, it is possible to prevent development of a void at the plating step.

[0018]

The removal step is preferably such a step at which the barrier

metal film is immersed in a mixture of a hydrofluoric acid and a nitric acid or a diluent of a hydrofluoric acid and the oxide film is selectively removed.

[0019]

The electroless plating step is preferably such a step at which the barrier metal film is immersed in a plating liquid which uses a glyoxylic acid as a reducer.

[0020]

The present invention may further comprise a step at which, through electrolytic plating which uses said electroless copper plating film as a seed layer, an electroless copper plating film is formed on said electroless copper plating film.

[0021]

[Preferred Embodiments of the Invention]

Preferred Embodiment 1

Fig. 1 shows cross sectional views of steps of manufacturing a multi-layer interconnection structure according to a preferred embodiment 1. In Fig. 1, the same reference symbols to those shown in Fig. 3 denote the same or corresponding portions. These manufacturing steps include the following steps 1 through 5.

[0022]

Step 1: As shown in Fig. 1(a), an inter-layer insulation film 3 of silicon oxide is formed on an inter-layer insulation film 1 which is made of silicon oxide and comprises a lower-layer wire 2. Next, the inter-layer insulation film 3 is etched, thereby forming a via hole (hole portion) 4.

[0023]

Following this, by a sputtering method, a barrier metal film (underlying metal) 5 of TaN is formed on the entire surface. As a sputtering gas, a mixture gas of Ar and N_2 is used. Sputtering conditions such as a nitrogen partial pressure are adjusted so that the element composition ratio (N / Ta) of the barrier metal film 5 will be controlled to be 0.3 or higher but 1.5 or lower, and more preferably, 0.3 or higher but 1.0 or lower. When the barrier metal film 5 is formed by sputtering in this manner, the film thickness on a side wall becomes thinner than the film thickness on a bottom portion of the via hole

4. When the film thickness on the bottom portion is about 10 nm, the film thickness on the side wall is about 2 nm.

[0024]

Fig. 2 shows a relationship between the time during which the barrier metal film 5 is left in atmosphere and the film thickness of the natural oxide film (TaOx) 6 formed on the surface of the barrier metal film in a condition that the element composition ratio (N / Ta) of the barrier metal film 5 of TaN is changed from 0 to 1.65.

As can be seen in Fig. 2, when N / Ta is 0.30, exposure to atmosphere for fifteen days makes the natural oxide film 6 grow into the film thickness of merely about 1 nm. During actual manufacturing steps, the barrier metal film 5 is exposed to atmosphere for as short a time as a few minutes, and hence, use of the barrier metal film 5 whose element composition ratio is such allows to control the film thickness of the natural oxide film 6 to 1 nm or less.

[0025]

When the element composition ratio (N / Ta) of the barrier metal film 5 is larger than 1.5, the electric resistance rate of TaN becomes extremely high. Hence, TaN preferably has an element composition ratio (N / Ta) of 1.5 or smaller, and more preferably, 1.0 or smaller, to be used as a material of wires.

In addition, although the foregoing has described that the barrier metal film 5 of TaN is formed by a sputtering method, the barrier metal film 5 of TaN may be formed by an ALD (Atomic Layer Deposition) method, a CVD method or the like.

[0026]

Step 2: As shown in Fig. 1(b), the barrier metal film 5 is exposed to atmosphere, whereby the surface of the barrier metal film 5 is oxidized and the natural oxide film 6 of TaN is formed. At this stage, the element composition ratio (N / Ta) of the barrier metal film 5 is controlled to be 0.3 or higher but 1.5 or lower. Due to this, the film thickness of the natural oxide film 6 which is formed as a consequence of oxidation of the barrier metal film 5 is about 1 nm or thinner.

As described above, since the film thickness of the barrier metal film 5 located at the side wall of the via hole 4 is about 2 nm, even when the natural oxide film 6 as thick as about 1 nm is formed, the

barrier metal film 5 which is not oxidized remains in the film thickness of about 1 nm on the side wall of the via hole 4.

[0027]

Step 3: As shown in Fig. 1(c), the natural oxide film 6 formed on the surface of the barrier metal film 5 is removed through etching. The etching uses a mixture of a hydrofluoric acid and a nitric acid or a diluent which is prepared by diluting a hydrofluoric acid with pure water ten or more times. This makes it possible to selectively remove the natural oxide film 6 alone without damaging the barrier metal film 5.

To be more specific, an aqueous solution mixed at a ratio of $HF : HNO_3 : H_2O = 1 : 1 : 30$ is used as an etchant. The etchant is set to a temperature of about 25℃, and the etching time is about three minutes. As shown in Fig. 1(c), this etching step leaves, the barrier metal film 5 from whose surface the natural oxide film 6 has been removed, on the bottom portion and the side wall of the via hole 4 and a top surface of the inter-layer insulation film 3.

[0028]

Step 4: As shown in Fig. 1(d), by means of immersion into a plating liquid which contains copper, electroless plating is executed. The plating liquid is comprised mainly of copper sulfate, a glyoxylic acid (reducer), ethylene diaminetetraacetate (complexing agent) and bipyridine (stabilizer). Plating conditions are, for instance, that pH of the solution is 12 and the temperature of the solution is 70℃.

Through such electroless plating, a uniform electroless copper plating film 7 as that shown in Fig. 1(d) is formed which defines a via hole which has the diameter of 100 nm and the aspect ratio (depth / diameter) of about 8. The film thickness of the electroless copper plating film 7 is about 10 nm

The adhesion between the barrier metal film 5 and the electroless copper plating film 7 is tight enough to ensure chemical and mechanical polishing (CMP).

[0029]

Step 5: As shown in Fig. 1(e), further, by an electrolytic plating method, an electrolytic copper plating film 8 is formed. The electrolytic plating uses a solution which is comprised mainly of copper

sulfate.

Through these steps, a multi-layer interconnection structure 100 is obtained whose via hole 4 is filled up with copper without any void as shown in Fig. 1(e).

[0030]

Preferred Embodiment 2

A method of manufacturing a multi-layer interconnection structure according to the preferred embodiment 2 of the present invention is different as for the step of forming the barrier metal film 5 (step 1) from but is otherwise similar to the manufacturing method according to the preferred embodiment 1 described earlier.

[0031]

In other words, the manufacturing method according to the preferred embodiment 2 first requires to form a Ta film by a sputtering or CVD method inside a vacuum chamber to eventually form the barrier metal 5 of TaN.

Following this, while maintaining the vacuum chamber at vacuum, nitrogen plasma is irradiated upon a surface of the Ta film, thereby turning an area near the surface of the Ta film into a TaN film. At this nitriding step, nitriding conditions are controlled such that the element composition ratio (N / Ta) of N to Ta within the TaN film will be 0.3 or higher but 1.5 or lower, and more preferably, 0.3 or higher but 1.0 or lower.

[0032]

To be more specific, after introducing nitrogen into the vacuum chamber and setting the vacuum chamber to 10 mTorr, inductively coupled plasma is generated. A direct current bias of about -50 V is applied upon a substrate which seats a wafer in which a multi-layer interconnection structure is to be formed. Under this condition, an area near the surface of the TaN film is nitrided.

Under this condition, such an TaN film is formed whose element composition ratio (N / Ta) of N to Ta is 0.3 or higher but 1.5 or lower at the depth of about 2 through 4 nm from the surface of the TaN film.

[0033]

As described in relation to the preferred embodiment 1, even after left in atmosphere for about two weeks, the TaN film having such

an element composition ratio grows a natural oxide film, which results from oxidation of the surface of the TaN film, into the film thickness of merely 1 nm or less (See Fig. 1(b).).

[0034]

As the steps 3 through 5 shown referred to for the preferred embodiment 1 (Figs. 1(c) through (e)) are carried out after this, the multi-layer interconnection structure 100 is obtained.

[0035]

Although the foregoing has described the preferred embodiments 1 and 2 as an example where TaN is used as the material of the barrier metal film 5, other TaN-containing material comprised mainly of Ta and N may be used instead.

[0036]

[Effect of the Invention]

As clearly described above, when the method of manufacturing a multi-layer interconnection structure according to the present invention is used, growth of a natural oxide film on a surface of a barrier metal film is suppressed. This makes it possible to form a buried interconnection in which development of a void is discouraged.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 shows cross sectional views of the steps of manufacturing a multi-layer interconnection structure according to the preferred embodiment 1 of the present invention.

[Fig. 2] Fig. 2 shows a relationship between the time during which a barrier metal film is left in atmosphere and the film thickness of a natural oxide film (TaOx) formed on the surface of the barrier metal film in a condition that the element composition ratio (N / Ta) of the barrier metal film is changed.

[Fig. 3] Fig. 3 shows cross sectional views of the conventional steps of manufacturing a multi-layer interconnection structure.

[Explanation of Keys]

1...inter-layer insulating film, 2...lower-layer wire, 3...inter-layer insulating film, 4...via hole, 5...barrier metal film, 6...native oxide film, 7...electroless copper plating film, 8... electrolytic copper plating film, 100 multi-layer interconnection structure

〔DOCUMENT NAME〕 DRAWINGS

Fig. 1

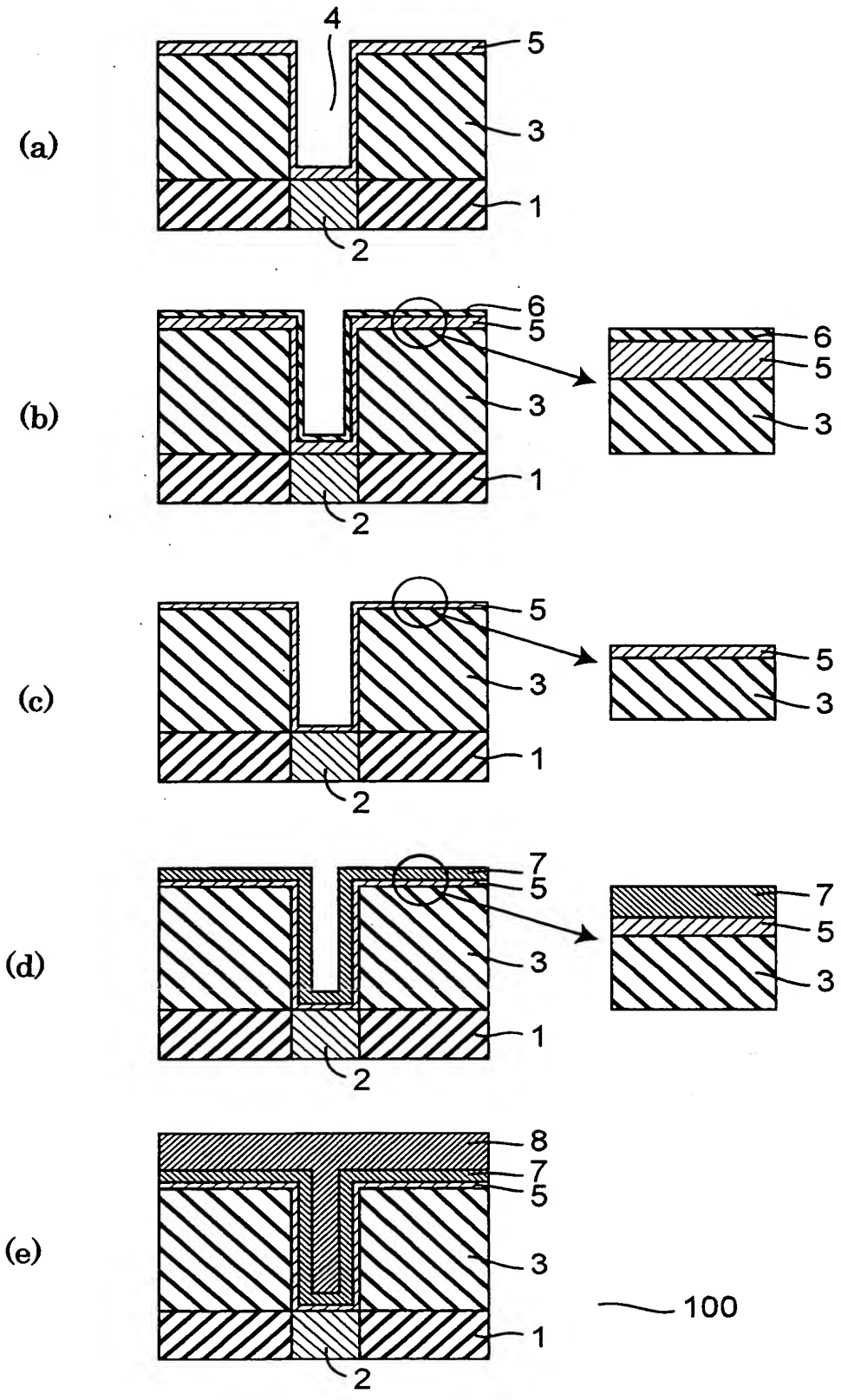
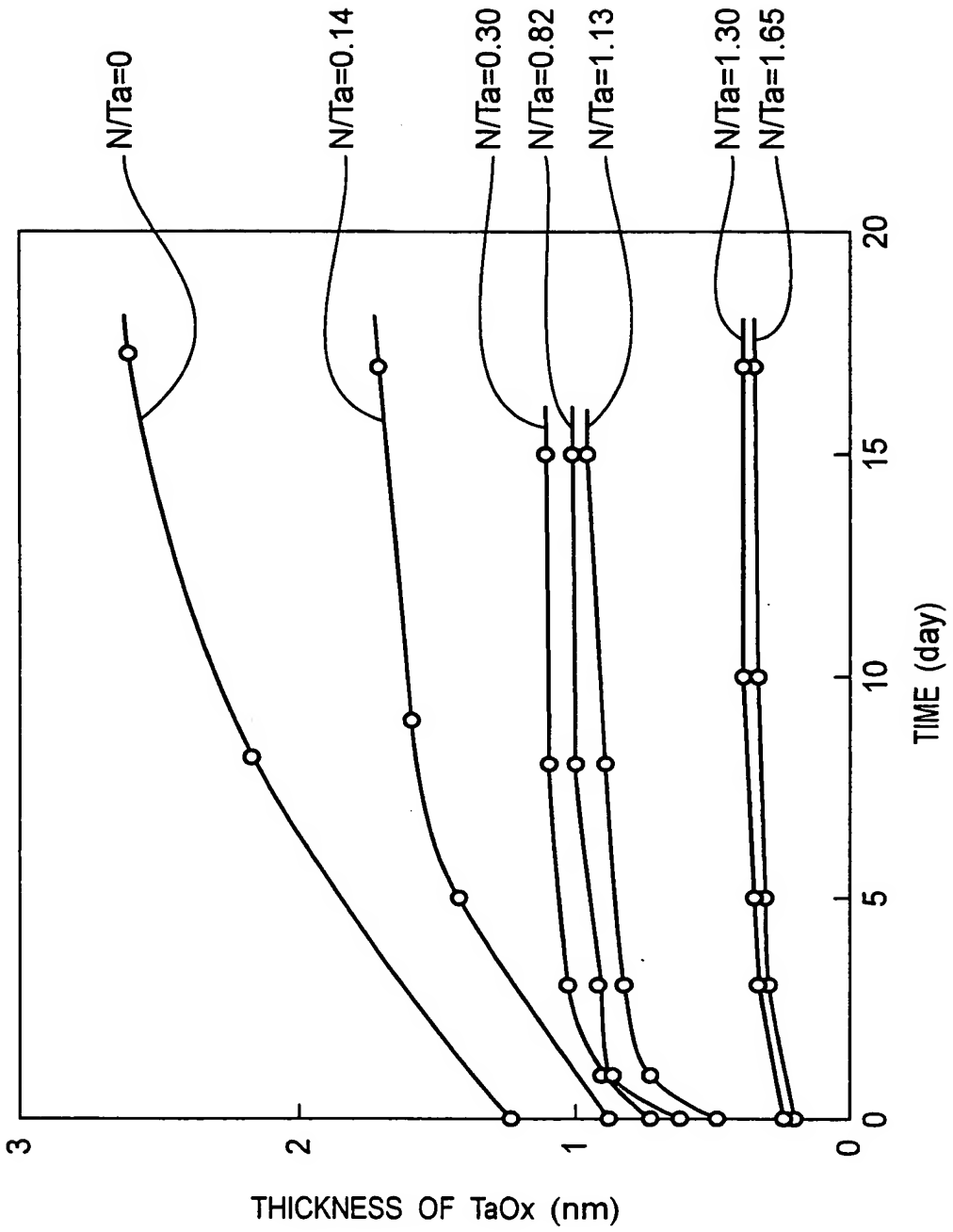


Fig.2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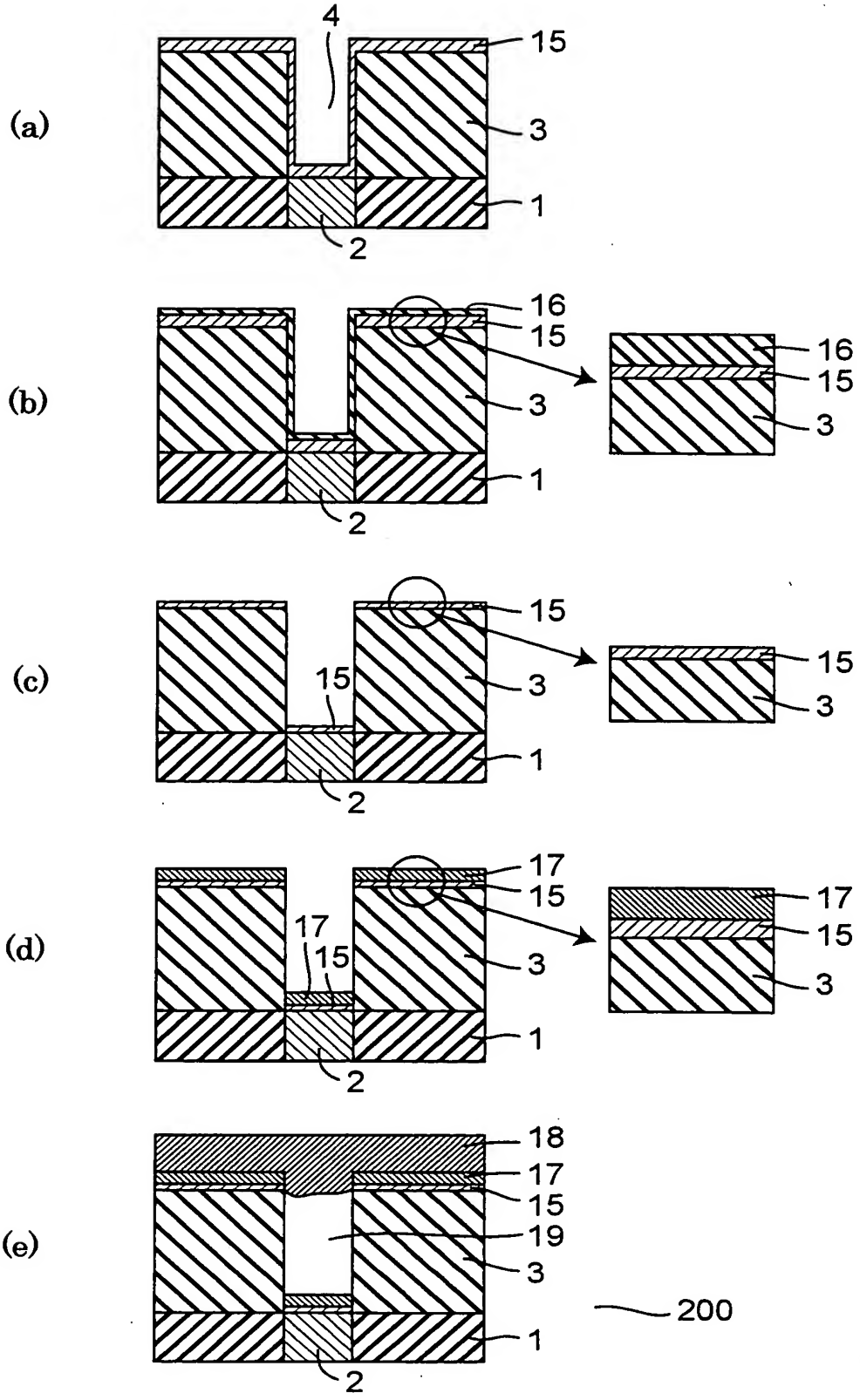
N/Ta=0.30
N/Ta=0.82
N/Ta=1.13
N/Ta=1.30
N/Ta=1.65
0
5
10
15
20
TIME (day)
0
1
2
3
THICKNESS OF TaOx (nm)

Fig.3


(a)
4
15
3
1
2
(b)
16
15
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2
16
15
3
(c)
15
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1
2
15
3
(d)
17
15
17
15
3
1
2
17
15
3
(e)
18
17
15
19
3
1
2
200

[Document Name] Abstract

[Abstract]

[Problem] Providing a method of manufacturing a multi-layer interconnection structure in which a natural oxide film formed on a surface of a barrier metal film is thin and development of a void is prevented.

[Means for Solving Problem] A method of manufacturing an embedded multi-layer interconnection structure, including: a step of forming a hole portion in an insulation layer; a barrier metal film forming step of forming a barrier metal film which is comprised mainly of tantalum and nitrogen in such a manner that the barrier metal film covers at least an inner wall of the hole portion; a removal step of removing an oxide film formed on a surface of the barrier metal film; and an electroless plating step of immersing the barrier metal film in a plating liquid containing copper and thereby forming an electroless copper plating film on the barrier metal film, characterized in that an element composition ratio (N / Ta) of nitrogen to tantalum contained in the barrier metal film is 0.3 or higher but 1.5 or lower.

[Selected Drawings] Fig. 1

Applicant Record

Identification No.: 396023993

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